CLAIMS

- 1. (Currently Amended) A memory module comprising:
- a <u>first</u> redrive circuit to receive a signal from a first point-to-point link and redrive the signal on a second point-to-point link;

a second redrive circuit to receive a second signal from a third point-to-point link and redrive the signal on a forth point-to-point link;

a memory device; and

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- a data accumulator coupled between the first redrive circuit and the memory device.
- 2. (Original) A memory module according to claim 1 wherein the point-to-point links comprise unidirectional links.
- 3. (Original) A memory module according to claim 1 wherein the data accumulator comprises a FIFO structure.
 - 4. (Cancelled)
- 5. (Currently Amended) A memory module according to claim 1 [[4]] wherein the memory device is coupled to the second redrive circuit.
- 6. (Original) A memory module according to claim 5 further comprising a second data accumulator coupled between the memory device and the second redrive circuit.
- 7. (Original) A memory module according to claim 1 wherein the memory device has a burst bandwidth that is greater than the bandwidth of the redrive circuit.
- 8. (Original) A memory module according to claim 1 wherein the data accumulator is constructed and arranged to accumulate data from the redrive circuit.
- 9. (Original) A memory module according to claim 1 wherein the data accumulator is constructed and arranged to accumulate data to the redrive circuit.

- 10. (Currently Amended) A memory buffer comprising:
- a <u>first</u> redrive circuit to receive a <u>first</u> signal from a first point-to-point link and redrive the signal on a second point-to-point link; and

a second redrive circuit to receive a second signal from a third point-to-point link and redrive the second signal on a fourth point-to-point link; and

a memory interface coupled to the <u>first</u> redrive circuit, wherein the memory interface comprises a data accumulator.

- 11. (Original) A memory buffer according to claim 10 wherein the point-to-point links comprise unidirectional links.
- 12. (Original) A memory buffer according to claim 10 wherein the data accumulator comprises a FIFO structure.
 - 13. (Cancelled)

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- 14. (Currently Amended) A memory buffer according to claim [[13]] 10 further comprising a second data accumulator coupled between the memory interface and the second redrive circuit.
 - 15. (Currently Amended) A memory system comprising:
 - a memory controller;
 - a memory agent having [[a]] first and second redrive circuits; and
- a first point-to-point link arranged to transmit a signal from the controller to the <u>first</u> redrive circuit of the memory agent;

wherein the memory agent comprises a data accumulator coupled to the <u>first</u> redrive circuit.

- 16. (Original) A memory system according to claim 15 wherein the point-to-point links comprise unidirectional links.
- 17. (Original) A memory system according to claim 15 wherein the data accumulator comprises a FIFO structure.

18. (Canceled)

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- 19. (Original) A memory system according to claim 15 further comprising a second point-to-point link arranged to transmit a signal from the memory agent to the controller.
 - 20. (Cancelled)
- 21. (Currently Amended) A memory system according to claim [[18]] <u>15</u> wherein the memory agent further comprises a second data accumulator coupled to the second redrive circuit.
 - 22. (Currently Amended) A method for operating a memory agent comprising: receiving a first signal on a first point-to-point link; redriving the first signal on a second point-to-point link; receiving a second signal on a third point-to-point link; redriving the second signal on a forth point-to-point link; accumulating write data from the first signal; and delivering the write data to a memory device.
- 23. (Original) A memory system according to claim 22 wherein the point-to-point links comprise unidirectional links.
- 24. (Original) A method according to claim 22 wherein accumulating and delivering the write data comprises accumulating and delivering the write data in a FIFO sequence.
 - 25. (Cancelled)
 - 26. (Original) A method according to claim 22 further comprising: accumulating read data from a memory device; and transmitting the read data as the second signal.

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